Title: HIGH SPEED SOFTWARE DRIVEN EMULATOR COMPRISED OF A PLURALITY OF EMULATION PROCESSORS WITH A METHOD TO ALLOW HIGH SPEED BULK READ/WRITE OPERATION SYNCHRONOUS DRAM WHILE REFRESHING THE MEMORY

Abstract of the Disclosure:

A system and method for bulk transfer to and from the SRAMs in which a starting memory address is latched and is then incremented every clock cycle to generate a new memory address. The addresses are decoded and memory requests are pipelined to the SRAM memory, one every clock cycle. When the memory controller detects transfer of the boundary of a predetermined number of clock cycles or words (e.g. 64 words or four clock cycles) the burst mode of data transfer is stopped and the memory controller waits for a "done" signal before resuming another cycle of the burst transfer mode. The memory controller on detecting a request on this address boundary first does a memory refresh followed by a requested operation; e.g. a continuation of the transfer operation.